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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,340	03/17/2004	Thomas Nulsen	NPT-65.0402	5585

7590 08/14/2006

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EXAMINER	
NGUYEN, HIEP	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 08/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/803,340	NULSEN ET AL.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,10-14 and 18-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-14* is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *19 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *attached drawing*.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4, 5 and 18 are rejected under 35 U.S.C. 102 (1, 4, 5 and b) as being anticipated by Yamamoto et al. (USP. 5,444,744). See attachment.

Regarding claim 1, figures 8 and 10A-10I of Yamamoto show a clock based voltage deviation detector comprising:

a pulse module (15b) having a pulse input for receiving a clock signal (J) and a pulse output for outputting a stream of reset pulses (B);

an indicator module (9a, 11, 12, 21) having a first indicator input for receiving an input signal (I4), a second indicator input for receiving a reference voltage (9b), a third indicator input communicatively coupled to said pulse output of said pulse module (15b) and an indicator output for outputting a pass/fail indicator signal (E) as a function of said stream of reset pulses (B) and a difference between an input signal (I4) and a reference voltage (9b), and

a correlation module (23, 24, 22, 25) having a first correlation input for receiving said clock signal (J) , a second correlation input communicatively coupled to said indicator output of said indicator module, wherein an event of said pass/fail indicator is correlated to a period of said clock signal at which said event occurred. Note that figure 10 shows that the pass/fail indicator (10E) correlates to clock (10B) and clock (10B) or clock (B) in figure (8) is the divided clock (J). Thus, the event of the pass/fail indicator (10E) correlates to clock (J).

Regarding claim 4, the indicator module comprises:

a comparator (9a) having a first comparator input for receiving said input signal, a second comparator input for receiving said reference voltage and a comparator

output for outputting a trip signal (K) as a function of a difference between said input signal and said reference; and

a latch (11) having a first input communicatively coupled to said comparator output of said comparator, a second input communicatively coupled to said pulse output (B) and a latch output for outputting said pass/fail indicator (K) as a function of said trip signal and said stream of reset pulses (B).

Regarding claim 5, figure 8 of Yamamoto shows a latch enable comparator (9a, 11) having first to third inputs receiving input signal (I4), reference voltage (9b) and pulse output (B) of the pulse module (15b).

Regarding claim 18, figure 8 shows a clock based voltage deviation detector comprising:

a means for generating a reset pulse stream as a function of a clock signal (15b);

a means for generating a pass/fail indicator signal as a function of said reset pulse stream and an event of a monitored voltage (9a, 11, 12, 21); and

a means for correlating an event of said pass/fail indicator signal with a specific period of said clock signal at which said event occurred (23, 24, 22, 25).

Allowable Subject Matter

Claims 10-14 are allowed because the prior art (US. 5,444,744) fails to teach or suggest a clock based voltage deviation detector comprising a counter and a storage module.

Claims 2, 3, 19 and 20 are objected to because the prior a fails to teach or suggest a Pulse module comprising a delay cell and an exclusive-OR gate as called for in claim 2; a correlation module comprising a counter and a storage module; clock based voltage deviation detector comprising a means for generating a reset pulse stream and a means for further generating the pass/fail indicator signal as called for in claim 19.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

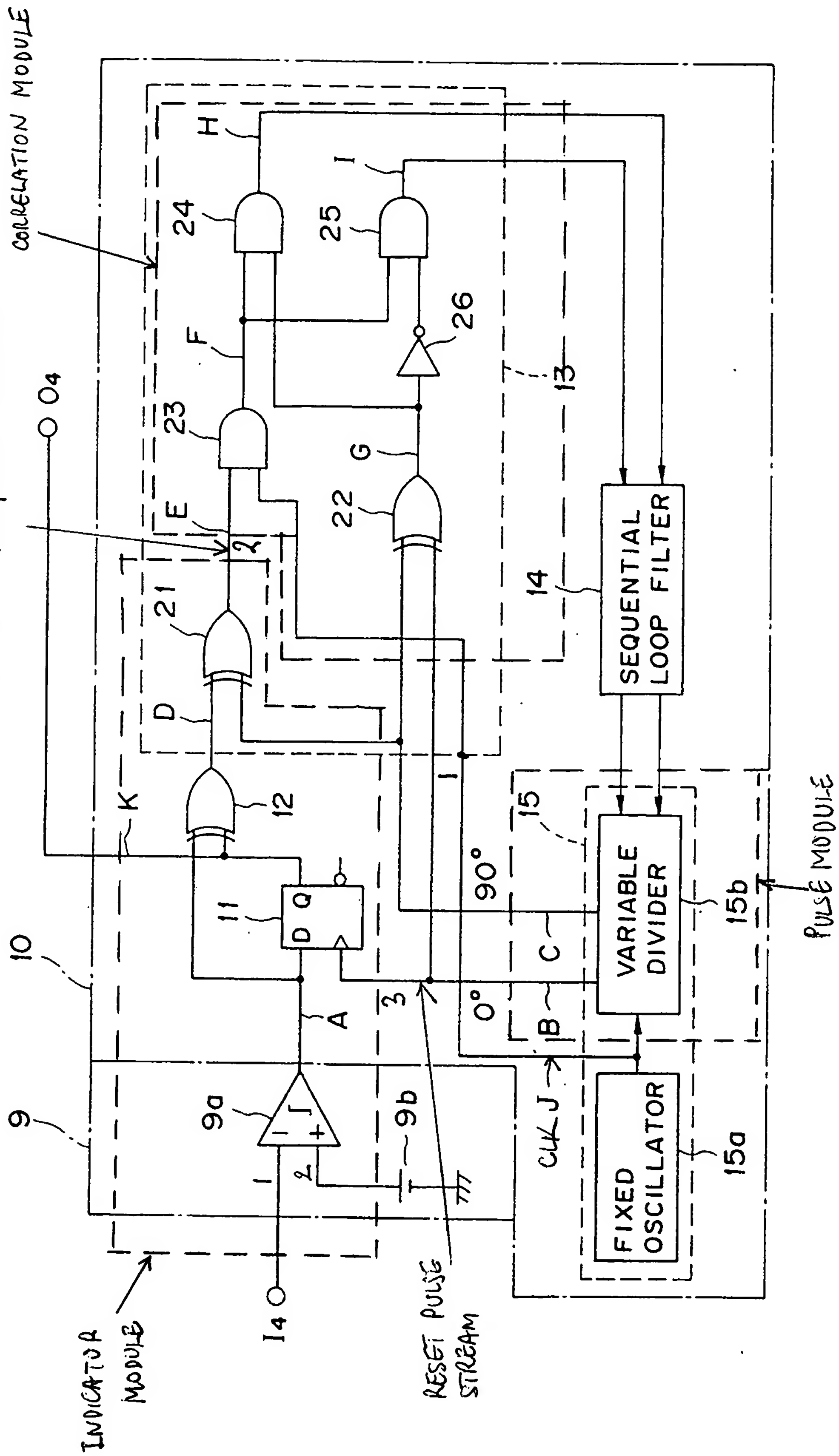
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Hiep Nguyen

08-03-06

TUAN T. LAM
PRIMARY EXAMINER

FIG 8


CORRELATION MODULE
PASS/FAIL INDICATOR
SEQUENTIAL LOOP FILTER
VARIABLE DIVIDER
FIXED OSCILLATOR
PULSE MODULE
INDICATOR MODULE
RESET PULSE STREAM
CLK J
90°
0°